BAJOPMAS JOURNAL 16(1): 27 – 38
Printed in Bayero University, Kano - Nigeria.

EVALUATION OF THE EFFECT OF GEOMETRICAL PARAMETERS ON SHORT CHANNEL EFFECTS IN NANOSCALE DOUBLE GATE FinFETs WITH COMPOUND SEMICONDUCTORS AS CHANNEL MATERIALS

[1*]Nura, M. S.; [1]Ali, M. H. and [1]Babaji, G.
[1]Department of Physics, Bayero University, Kano, Nigeria.
*Corresponding author (Email: nmshehu.phy@buk.edu.ng.)

ABSTRACT
The quest for smaller transistors centers on nanoscale technology, which drives major breakthroughs in semiconductors by enabling hundreds of circuits on a chip through Very Large Scale and Ultra-Large Scale Integrations. However, reducing device dimensions generate short channel effects, (SCEs) in MOSFETs, which negatively affect its performance. This study evaluates the influence of key geometrical parameters; gate oxide thickness, channel length, and channel width on short channel effects (SCEs) in nanoscale double-gate FinFETs. The critical SCEs examined include Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), and Threshold Voltage (Vth) roll-off. FinFETs designed from Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN), and Silicon (Si) were analyzed using the PADRE simulator. The Results reveal that reducing gate oxide thickness is essential for minimizing DIBL and SS, with GaAs-FinFET achieving the lowest DIBL (4.38 mV/V) and Si-FinFET demonstrating the lowest SS (80.54 mV/dec) at 2 nm thickness. GaSb-FinFET outperforms others in threshold voltage, with the lowest Vth (0.33 V) at 14 nm thickness. Moreover, an optimal channel length of 45 nm effectively mitigates DIBL and SS, where GaAs-FinFET records the lowest DIBL (1.52 mV/V) and Si-FinFET exhibits the lowest SS (77.26 mV/dec). GaSb-FinFET achieves the lowest threshold voltage at 20 nm channel length. Additionally, channel width significantly affects SCEs, with an optimal width of 10 nm reducing these effects. At this width, (10 nm), GaAs-FinFET records the lowest DIBL of 4.38 mV/V, Si-FinFET achieves the lowest SS of 90.88 mV/dec, and GaN-FinFET demonstrates the lowest Vth (0.36 V). These findings underscore the importance of optimizing geometrical parameters to enhance FinFET performance and mitigate short channel effects, paving the way for improved nanoscale device design.

Keywords: DIBL, FinFETs, Geometrical Parameters, GaAs, GaSb, SCEs

1.0 Introduction
The desire for transistor miniaturization serves as a cornerstone of nanoscale technology, playing a pivotal role in revolutionizing the semiconductor industry [1–7]. This progress has paved the way for the integration of hundreds, and in some cases thousands, of circuits onto a single chip through advanced methodologies like Very Large-Scale Integration (VLSI) and Ultra-Large-Scale Integration (ULSI). These integrations have significantly enhanced the performance, functionality, and efficiency of modern electronic devices. However, as the dimensions of transistors shrink, they face inherent challenges that hinder their operation, particularly in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). These challenges, collectively referred to as short channel effects (SCEs) [8–14], arise due to the reduced control of the gate over the channel as the channel length decreases. SCEs lead to undesirable effects such as increased leakage currents, threshold voltage roll-off, and degraded device performance, posing a significant obstacle to further scaling. To address these limitations, the Fin Field Effect Transistor (FinFET) has emerged as a cutting-edge solution [15–30]. This innovative structure provides better electrostatic control over the

channel compared to traditional planar MOSFETs. Its improved scalability, reduced leakage currents, and enhanced suppression of SCEs make the FinFET a promising candidate for next-generation electronic devices, ensuring continued progress in nanoscale technology.

Several researches have been conducted to examine short channel effects in FinFETs. Authors in [31]investigated short channel effects in n-FinFETs with Si, GaSb, GaN, and GaAs to determine the best channel material for double gate FinFETs. However, this study lacks an examination of some critical performance metrics such as oxide thickness for the various channel materials, limiting the overall device performance assessment. A comparative study [32] looked at double gate n-FinFET devices using Si, Ge, and GaAs channel materials, taking into consideration various short channel effects. The study looked at the effect of varied drain and gate voltages on device performance, with GaAs outperforming other materials in simulations. This study was based on FinFET operating conditions without taking the dimensional parameters' effect into account. The variability of various parameters like on-off current ratio, sub threshold slope and DIBL with variations in gate length were explored in [33]. The authors demonstrated that shorter gate lengths improved the performance of the FinFET. Effect of downscaling channel dimensions on performance characteristics of InAs-FinFET was studied in [34]. The authors demonstrated that low values of the InAs-FinFET dimensions were found to enhance the performance of the device. However, the impact of geometrical parameters, including gate oxide thickness, fin (channel) length, and fin (channel) width, on these short channel effects remains a critical challenge for optimizing the performance of nanoscale double-gate FinFETs. Additionally, the choice of channel materials such as GaAs, GaSb, GaN, and Si further complicates the relationship between geometry and device performance. There is a need for a comprehensive study that evaluates how variations in these parameters influence the short channel effects and overall efficiency of FinFETs, particularly with compound semiconductors as channel materials.

The aim of this research is to evaluate the effect of key geometrical parameters: gate oxide thickness, fin (channel) length, and fin (channel) width on short channel effects: drain-Induced barrier lowering, Subthreshold Swing, and threshold voltage roll-off, in nanoscale double-gate FinFETs. This study will also explore the performance of FinFETs with different channel materials, namely GaAs, GaSb, GaN, and Si, to determine their suitability for mitigating short channel effects and enhancing device efficiency. The analysis will be carried out in the PADRE Simulator, known for semiconductor device modeling. Understanding these effects is crucial for advancing the design of highly efficient, low-power, and high-performance FinFET devices for next-generation nanoelectronics applications.

2. Theoretical Background

This section discusses the FinFET device structure and short channel effects.

2.1 Device Structure

Figure 1 illustrates a 2-dimensional double gate FinFET structure used in this simulation.

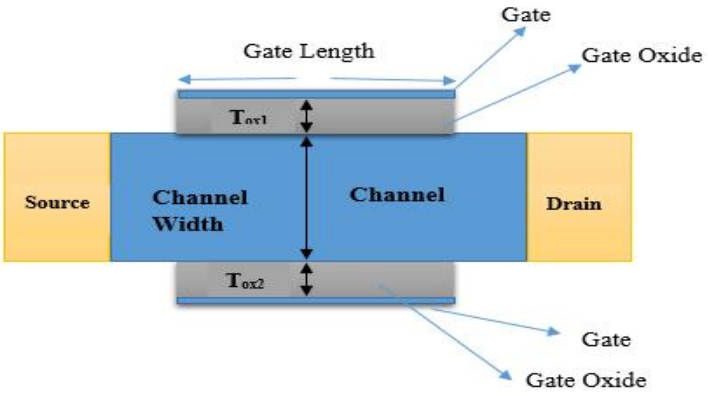

Figure 1: Two-Dimensional FinFET Structure.

The FinFET is characterized by its conducting channel being encircled by a thin silicon "fin" that serves as the device's body. The device has crucial body parts such as source, drain, gate length (also called channel length), and channel width (also called fin width or fin thickness). There is an oxide with oxide thickness T_{ox1} and T_{ox2} placed on top surface of the fin on each side wall [31]. The basic idea behind the FinFET construction is to bring the gate capacitance near FinFET channel. The fin body is typically quite narrow, giving the gate superior control over the channel. To accomplish this, the silicon body is very thin, ensuring that no leakage path is too distant from one of the gates, hence lowering leakage current. Because the channel is regulated by two or more gates, they provide more control over the channel [35].

2.2 Short Channel Effects

Scaling down MOSFET introduced some problems that lead to performance deterioration. These problems are called short channel effects. Short channel effects include the following:

Drain Induced Barrier Lowering

The increase in drain voltage from 0.01 V to 0.05 V causes a variation in threshold voltage. This is referred to as drain induced barrier lowering. It is one of the most critical short channel effects. The DIBL value can be determined using [36]:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_{DS}} \tag{1}$$

where V_{TH} denotes threshold voltage and V_{DS} denotes drain-source voltage.

Subthreshold Swing

The subthreshold swing parameter, one of the SCEs, for a Multigate Field Effect Transistor is usually 60 mV/dec. The SS can be calculated by [37]:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS}\ )} \tag{2}$$

where V_{GS} denotes gate-source voltage and I_{DS} denotes drain-source current.

Threshold Voltage

Assessing the threshold voltage of a device is a crucial step in determining its feasibility as a channel material for switching applications. The lowest gate voltage required to provide a conduction path between the source and the drain is known as the threshold voltage [14]. The threshold voltage can be calculated [12]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (3)$$

Where Q_{SS} denotes gate dielectric charge, C_{ox} is the capacitance in the gate, Q_D is the channel depletion charge, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential, and V_{in} is the additional surface potential to $2f_f$ that is required for ultrathin body devices to cause enough inversion charges in to the channel region of the transistor to reach threshold point [12].

3.0 Methodology

The device simulation was performed using the PADRE simulator from the MuGFET tool. We investigated the effect of FinFET's geometrical parameters on short channel effects. Specifically, The FinFETs simulated were GaAs-FinFET, GaSb-FinFET, GaN-FinFET and Si-FinFETs. The key short channel effects analyzed were drain-induced barrier lowering, subthreshold swing and threshold voltage roll-off. During the simulation, the drain/source doping was set at 1×10^{16} cm^{-3} and the channel doping concentration was maintained at 1×10^{19} cm^{-3}. While the gate bias was set between 0 V and 1 V, and the drain bias was set at and 1 V. The oxide thickness was varied at 2 nm, 4 nm, 6 nm, 8 nm, 10 nm, 12 nm and 14 nm, the fin (channel) was varied at 20 nm, 25 nm, 30 nm, 35 nm, 40 nm, 45 nm, 50 nm, the fin (channel) width was varied from 10 nm to 15nm, 20 nm, 25 nm, 30 nm, 35 nm and 40 nm. The simulation was carried out at the temperature of 300 K.

4.0 Results and Discussion

This section presnts and discusses the results for the evaluation of the effect of geometrical parameters; fin(channel) length, fin width and oxide thickness on the short channel effects; drain-induced barrier lowering, subthreshold swing and threshold voltage roll-off in nanoscale double gate GaAs-FinFET, GaSb-FinFET, GaN-FinFET and Si-FinFET.

4.1 Effect of Gate Oxide Thickness on Drain-Induced Barrier Lowering

Figure 2 shows the graph of DIBL versus gate oxide thickness for GaAs-FinFET, GaSb-FinFET, GaN-FinFET, and Si-FinFET as fin (channel) materials. It can be observed from the figure that DIBL increases as the gate oxide thickness increases in all the four FinFETs. From 2 nm to 4 nm oxide thickness, the DIBL characteristics of the four FinFETs are nearly identical, indicating their interchangeability within this range. At 2 nm, all four FinFETs demonstrate low DIBL values, with GaAs-FinFET achieving the lowest DIBL value of 4.38 mV/V, showing its superior performance. On the other hand, Si-FinFET exhibits the highest DIBL value of 210.34 mV/V at 14 nm, indicating its poor performance in this aspect. These findings suggest that maintaining a low gate oxide thickness is critical for achieving low DIBL and enhancing FinFET performance.

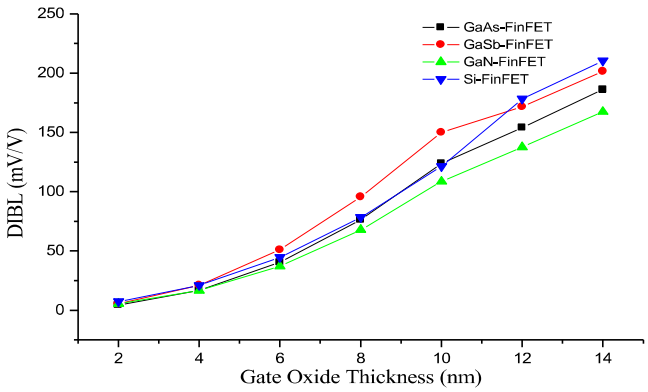

Figure 2:Graph of DIBL against Gate Oxide Thickness

4.2 Effect of Gate Oxide Thickness on Subthreshold Swing

Figure 3 shows the relationship between subthreshold swing (SS) and gate oxide thickness for nanoscale double-gate FinFETs based on GaAs, GaSb, GaN, and Si. The results demonstrate that SS increased as the gate oxide thickness increased from 2 nm to 6 nm across all four FinFET types. Beyond 6 nm, SS decreased up to 8 nm for GaAs-FinFET, GaSb-FinFET, and GaN-FinFET; however, for Si-FinFET, SS continued to increase up to 8 nm. For GaAs-FinFET, GaSb-FinFET, and GaN-FinFET, SS was observed to rise again as the oxide thickness extends from 8 nm to 14 nm. At a gate oxide thickness of 2 nm, all four FinFETs achieved their lowest SS values, identifying this thickness as the optimal point for their performance. Notably, the Si-FinFET exhibited the lowest SS value of 80.54 mV/dec at 2 nm, showcasing its superior performance at this thickness. In contrast, the highest SS value of 188.54 mV/dec was observed in the GaSb-FinFET at a gate oxide thickness of 14 nm, making it the least effective device in terms of SS.

These findings highlight the critical role of maintaining a low gate oxide thickness in achieving a reduced subthreshold swing, which is essential for enhancing the overall performance of FinFET devices. The results suggest that optimizing gate oxide thickness is a key factor in minimizing SS and improving FinFET efficiency.

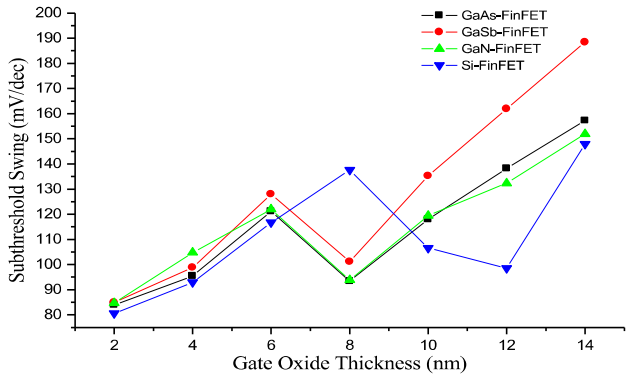

Figure 3: Graph of Subthreshold Swing against Gate Oxide Thickness

4.3 Effect of Gate Oxide Thickness on Threshold Voltage

Figure 4 shows the relationship between threshold voltage and gate oxide thickness for GaAs-FinFET, GaSb-FinFET, GaN-FinFET, and Si-FinFET. It can be observed from the figure that, the threshold voltage decreases as the gate oxide thickness increases for all four FinFETs. At an oxide thickness of 14 nm, the threshold voltage is low in all the four FinFETs, with GaSb-FinFET achieving the lowest value of 0.37 V, demonstrating superior performance compared with the other three devices. In contrast, Si-FinFET exhibits the highest threshold voltage of 0.53 V, making it the least efficient among the four FinFETs. This observation suggests that a higher gate oxide thickness is essential for enhancing FinFET performance concerning threshold voltage.

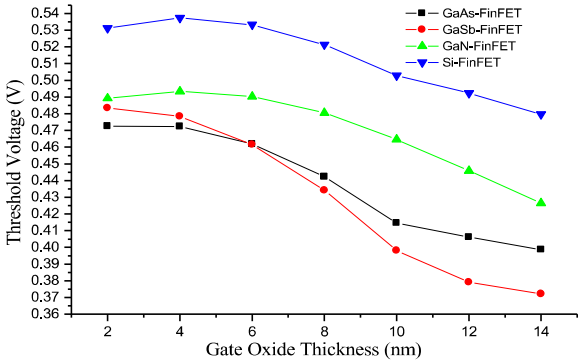

Figure. 4: Graph of Threshold Voltage against Gate Oxide Thickness

4.4 Effect of Fin (Channel) on Drain-Induced Barrier Lowering

The relationship between DIBL and Fin (channel) length is shown in Figure 5. It can be seen from the figure that DIBL decreases with the increase in the fin(channel) length of the GaAS-FinFET, GaSb-FinFET, GaN-FinFET and Si-FinFET from 20 nm to 45 nm, thereafter the DIBL continues to increase up to 50 nm. GaN-FinFET and GaAs-FinFET can be used interchangeably between the channel length of 45 nm and 50 nm. It can be observed that all the four exhibit low DIBL at the channel length of 45 nm with GaAs-FinFET showing lowest DIBL value of 1.52 mV/V at the channel length of 45 nm. This finding suggests that maintaining the channel length of the FinFET at 45 nm will keep low DIBL for enhanced FinFET performance.

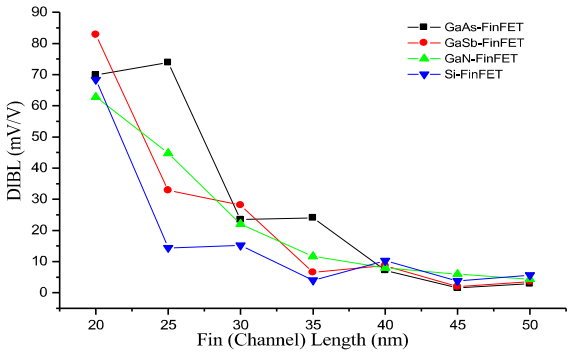

Figure 5: Graph of DIBL against Fin (Channel) Length

4.5 Effect of Fin (Channel) length on Subthreshold Swing

Figure 6 shows the variation of subthreshold swing with fin (channel) length for GaAs-FinFET, GaSb-FinFET, GaN-FinFET, and Si-FinFET. The graph highlights how DIBL behaves as the channel length increases from 20 nm to 50 nm. Initially, DIBL shows a decreasing trend as the channel length increases from 20 nm to 25 nm, signifying improved control over short channel effects within this range. However, beyond 25 nm, DIBL begins to rise at a channel length of 30 nm for GaAs, GaSb, and GaN FinFETs. Interestingly, Si-FinFET deviated from this trend, where its DIBL continued to rise, up to the channel length of 35 nm. Moreover, the graph shows that all the FinFETs exhibited low subthreshold swing values at a channel length of 45 nm, demonstrating enhanced device performance at this

dimension. Notably, the Si-FinFET outperformed the other devices by achieving the lowest subthreshold swing value of 77.26 mV/dec, highlighting its superior electrostatic control and energy efficiency at this channel length. This makes Si-FinFET the most efficient among the four FinFET devices in terms of subthreshold swing performance.

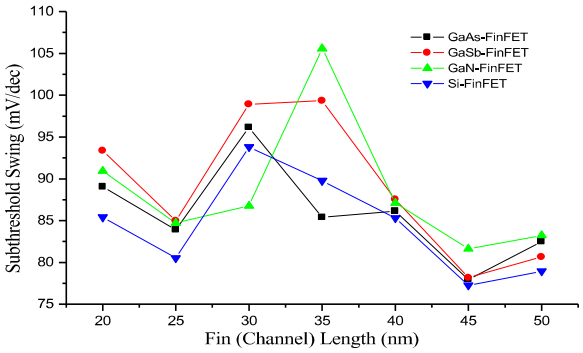

Figure 6: Graph of Subthreshold Swing against Fin (Channel) Length

4.6 Effect of Fin (Channel) Length on Threshold Voltage

Figure 7 shows the graph of threshold voltage versus channel length for GaAs-FinFET, GaSb-FinFET, GaN-FinFET, and Si-FinFET. The results show that the threshold voltage increases as the channel length grows from 20 nm to 35 nm, then decreases slightly from 35 nm to 40 nm before rising again up to 50 nm across all FinFETs. Notably, the threshold voltage remains relatively stable between 20 nm and 25 nm in GaAs-FinFET. Among the FinFETs, GaSb-FinFET exhibits the lowest threshold voltage of 0.33 V, indicating its superior performance at 20 nm. Conversely, Si-FinFET demonstrates the highest threshold voltage of 0.54 V at a channel length of 50 nm, making it the least efficient in terms of performance at this channel length. This finding highlights GaSb-FinFET's advantage in achieving better performance with low threshold voltage.

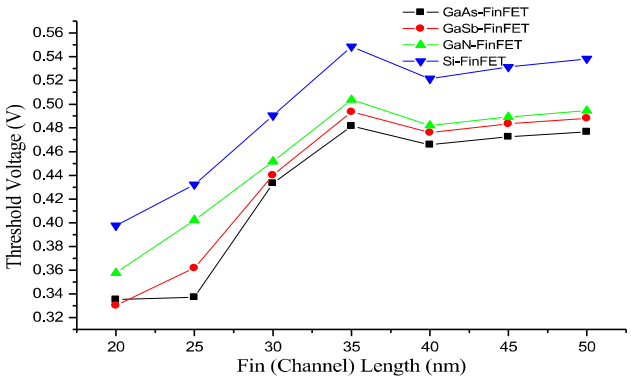

Figure 7: Graph of Threshold Voltage against Fin (Channel)

4.7 Effect of Fin (Channel) Width on Drain-Induced Barrier Lowering

The relationship between DIBL and channel width is shown in Figure 8 for GaAs-FinFET, GaSb-FinFET, GaN-FinFET and Si-FinFET. It can be seen from the figure that DIBL

increases as the channel width increases from 10 nm to 50 nm in all the four FinFETs. It was observed that the four FinFETs showed low DIBL at 10 nm with GaAs-FinFET exhibiting the lowest DIBL value of 4.38 mV/V at the same channel width. Comparing the four FinFETs, GaAs-FinFET exhibited much better performance in terms of DIBL than the other three FinFETs. On the other hand GaSb-FinFET showed worst performance with the highest DIBL value of 83.23 mV/V. This finding highlights that low channel width should be maintained for low DIBL to ensure enhanced FinFET performance.

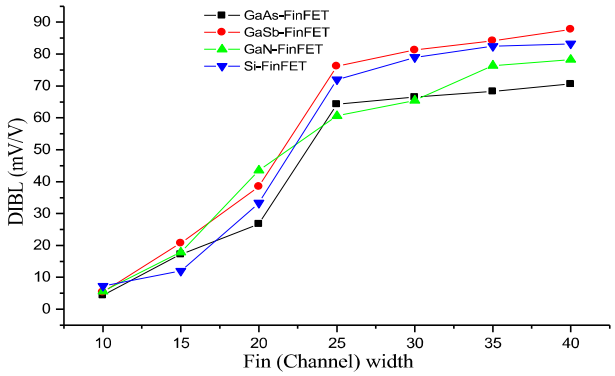

Figure 8: Graph of DIBL against Fin (Channel) Length

4.8 Effect of Fin (Channel) Length on Subthreshold Swing

Figure 9 shows the graph of subthreshold wing against channelwidth for GaAs-FinFET, GaSb-FinFET, GaN-FinFET and Si-FinFETs. It can be observed from the figure that subthreshold swing increases as the channel width increases from 10 nm to 20 nm channel widths after which it decreases between 20 nm and 25 nm channel widths in GaAs-FinFET, GaSb-FinFET and GaN-FinFET. The subthreshold swing continues to increase again from 25 nm to 40 nm channel widths. However, the subthreshold swing increases as the the channel width incraeses from 10 nm to 40 nm. It was observed that all the four FinFETs showed low subthreshold swing at the channel width of 10 nm, with Si-FinFET exhibiting lowest subthreshold value of 90.88 mV/dec. Hence Si-FinFET showed superior performance characteristics in terms of subthreshold swing. On the other hand, Si-FinFET also exhibited the highest subthreshold swing value of 161.35 mV/dec at the channel width of 40 nm. This finding highlights that in comparison with the other three FinFETs, Si-FinFET can have superior and worst subthreshold swing characteristics at low and high subthreshold swing.

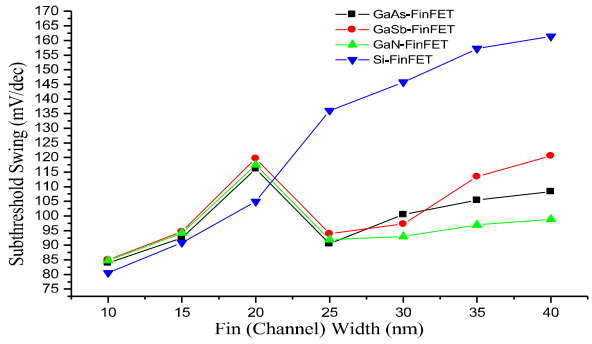

Figure 9: Graph of Subthreshold Swing against Fin (Channel) Length

4.9 Effcet of Fin (Channel) Length on Threshold Voltage

Figure 10 shows the relationship between threshold voltage and channel width for GaAs-FinFET,GaSb-FinFET, GaN-FinFET and Si-FinFET. It can be seen from the figure that there is increase and decrease in the threshold voltage in all the four FinFETs across the cahnnel widths under consideration. Among the FinFETs, GaN-FinFET exhibited much better threshold voltage characteristics at 10 nm with the lowest threshold voltage of 0.36 V. On the other hand Si-FinFET showed worst threshold voltage characteristics having the highest threshold voltage of 0.53 V.

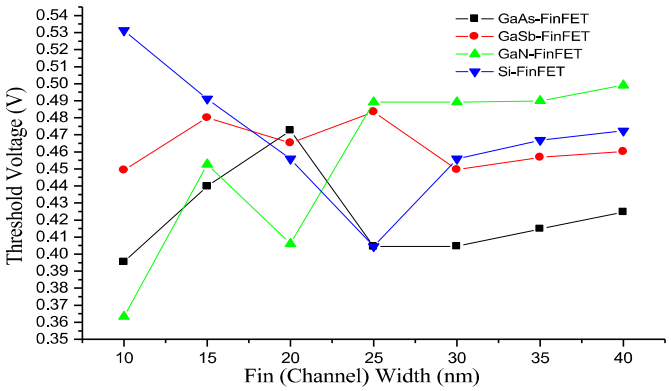

Figure 10: Graph of Threshold Voltage against Fin (Channel) Width

5. Conclusion

This study highlights the critical role of geometrical parameters; gate oxide thickness, channel length, and channel width in mitigating short channel effects (SCEs) in nanoscale double-gate FinFETs. The findings revealed that reducing gate oxide thickness is essential for minimizing Drain-Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS), while optimizing channel length and width significantly improves threshold voltage stability. GaAs-FinFET, GaSb-FinFET, GaN-FinFET, and Si-FinFET exhibited varying performance advantages depending on the specific SCE. The results emphasized that carefully tuning these parameters enhances device reliability and overall efficiency. These findings underscore the importance of careful device engineering to ensure high-performance, energy-efficient transistors for future semiconductor technologies. Further research can be carried out by utilizing machine learning algorithms to predict optimal device parameters, enhance modeling accuracy, and accelerate FinFET design and simulation processes.

References

[1] S. K. Dargar and V. M. Srivastava, “Performance Analysis of 10 nm FinFET with Scaled Fin-Dimension and Oxide Thickness,” *2019 Int. Conf. Autom. Comput. Technol. Manag. ICACTM 2019*, pp. 1–5, 2019, doi: 10.1109/ICACTM.2019.8776710.

[2] S. Mangesh, P. K. Chopra, and K. K. Saini, “Quantum effect in Nanoscale SOI FINFET device structure: A simulation study,” *Proc. 2nd Int. Conf. 2017 Devices Integr. Circuit, DevIC 2017*, pp. 795–798, 2017, doi: 10.1109/DEVIC.2017.8074062.

[3] P. Wambacq, B. Verbruggen, K. Scheir, J. Borremans, M. Dehan, D. Linten, V. D. Heyn, G. V. Plas, A. Mercha, V. Parvais, C. Gustin, V. Subramanian, N. Collaert, M. Jurczak and S. Decoutere, “The potential of FinFETs for analog and RF circuit applications,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 54, no. 11 SPEC. ISS., pp. 2541–2551,

2007, doi: 10.1109/TCSI.2007.907866.
[4] E. H. Minhaj, S. R. Esha, M. M. R. Adnan, and T. Dey, "Impact of Channel Length Reduction and Doping Variation on Multigate FinFETs," *2018 Int. Conf. Adv. Electr. Electron. Eng. ICAEEE 2018*, pp. 1–4, 2019, doi: 10.1109/ICAEEE.2018.8642981.
[5] S. Zhang, "Review of Modern Field Effect Transistor Technologies for Scaling," *J. Phys. Conf. Ser.*, vol. 1617, no. 1, 2020, doi: 10.1088/1742-6596/1617/1/012054.
[6] K. VinayakPrakash, A. Kumar, and P. Jain, "Circumventing Short Channel Effects in FETs: Review," *Int. J. Comput. Appl.*, vol. 117, no. 17, pp. 24–30, 2015, doi: 10.5120/20648-3407.
[7] D. Bhattacharya and N. K. Jha, "FinFETs: From devices to architectures,"*Advances in Electronics*, vol. 2014, pp. 21–55, 2015, doi: 10.1017/CBO9781316156148.003.
[8] R. M. Asif, S. U. Rehman, A. U. Rehman, M. Bajaj, S. Choudhury, and T. P. Dash, "A Comparative Study of Short Channel Effects in 3-D FinFET with High-K Gate Di-electric," *2021 Int. Conf. Adv. Power, Signal, Inf. Technol. APSIT 2021*, no. December, 2021, doi: 10.1109/APSIT52773.2021.9641388.
[9] Ameer F. Roslan, F. Salehuddin, A.S.M. Zain, K.E. Kaharudin, H. Hazura, A.R. Hanim, S.K. Idris, B.Z. Zarina, and Afifah Maheran A.H, "30nm DG-FinFET 3D construction impact towards short channel effects," *Indones. J. Electr. Eng. Comput. Sci.*, vol. 12, no. 3, pp. 1358–1365, 2018, doi: 10.11591/ijeecs.v12.i3.pp1358-1365.
[10] G. Saini and A. K Rana, "Physical Scaling Limits of FinFET Structure: A Simulation Study," *Int. J. VLSI Des. Commun. Syst.*, vol. 2, no. 1, pp. 26–35, 2011, doi: 10.5121/vlsic.2011.2103.
[11] M. Kailasam and M. Govindasamy, "Impact of high-k gate dielectrics on short channel effects of dg n-finfet," *Int. J. Sci. Technol. Res.*, vol. 9, no. 3, pp. 2023–2026, 2020.
[12] M. Mustafa, T. A. Bhat, and M. R. Beigh, "Threshold Voltage Sensitivity to Metal Gate Work-Function Based Performance Evaluation of Double-Gate n-FinFET Structures for LSTP Technology," *World J. Nano Sci. Eng.*, vol. 03, no. 01, pp. 17–22, 2013, doi: 10.4236/wjnse.2013.31003.
[13] G. R. Murthy, S. Tiwari, and S. Marasu, "IMPACT OF DIELECTRIC MATERIALS ON FinFET CHARACTERISTICS AT 45nm USING SILVACO ATLAS 2-D SIMULATIONS," *Sci.Int.(Lahore)*, vol. 33, no. 1, pp. 61–64, 2021.
[14] S. Banerjee, E. Sarkar, and A. Mukherjee, "Effect of Fin Width and Fin Height on Threshold Voltage for Tripple Gate Rectangular FinFET," *TTIC*, vol. 2, pp. 27–30, 2018.
[15] D. S. Bhargava, M. Sarumathi, and P. Venkatesh, "FinFET Technology : A Comparative Review of Traditional Transistors and FinFET based on performance metrics and physical dimensions," *Int. Journ. of Sci. Res in Comp. Sci. App. and Man. Stud.,* vol. 5, no. 6, 2016.
[16] Y. K. Ã, K. Tsutsui, K. Kakushima, P. Ahmet, V. R. Rao, and H. Iwai, "Analysis of Threshold Voltage Variation in Fin Field Effect Transistors : Separation of Short Channel Effects,"*Japanese Journal of Applied Physics,* vol. 044201, doi: 10.1143/JJAP.49.044201.
[17]Toshifumi Irisawa, Kimitoshi Okano, Takuya Horiuchi, Hiroshi Itokawa, Ichiro Mizushima, Koji Usuda, Tsutomu Tezuka, Naoharu Sugiyama, and Shin-ichi Takagi, "Electron mobility and short-channel device characteristics of SOI FinFETs with uniaxially strained (110) channels," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1651–1658, 2009, doi: 10.1109/TED.2009.2024029.
[18] C.-H. Lin, R. Kambhampati, R. J. Miller, T. B. Hook, A. Bryant, W. Haensch, P. Oldiges, I. Lauer, T. Yamashita, V. Basker, T. Standaert, K. Rim, E. Leobandung, H. Bu, and M. Khare "Channel doping impact on FinFETs for 22nm and beyond," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 15–16, 2012, doi: 10.1109/VLSIT.2012.6242438.

[19] C. R. Manoj and R. Rao, "Impact of high-k gate dielectrics on the device and circuit performance of nanoscale FinFETs," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 295–297, 2007, doi: 10.1109/LED.2007.892365.
[20] M. Poljak, V. Jovanović, and T. Suligoj, "Modeling study on carrier mobility in ultra-thin body FinFETs with circuit-level implications," *Solid. State. Electron.*, vol. 65–66, no. 1, pp. 130–138, 2011, doi: 10.1016/j.sse.2011.06.039.
[21] M. K. Rai, V. Narendar, and R. A. Mishra, "Significance of variation in various parameters on electrical characteristics of FinFET devices," *SCES 2014 Inspiring Eng. Syst. Glob. Sustain.*, vol. 1, pp. 2–7, 2014, doi: 10.1109/SCES.2014.6880096.
[22] V. Subramanian *et al.*, "Impact of fin width on digital and analog performances of n-FinFETs," *Solid. State. Electron.*, vol. 51, no. 4 SPEC. ISS., pp. 551–559, 2007, doi: 10.1016/j.sse.2007.02.003.
[23] R. S. Pal, S. Sharma, and S. Dasgupta, "Recent trend of FinFET devices and its challenges: A review," *2017 Conf. Emerg. Devices Smart Syst. ICEDSS 2017*, no. March, pp. 150–154, 2017, doi: 10.1109/ICEDSS.2017.8073675.
[24] Z. Lu and J. G. Fossum, "Short-channel effects in independent-gate FinFETs," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 145–147, 2007, doi: 10.1109/LED.2006.889236.
[25] A. Kumar and S. S. Singh, "Optimizing FinFET parameters for minimizing short channel effects," *Int. Conf. Commun. Signal Process. ICCSP 2016*, pp. 1448–1451, 2016, doi: 10.1109/ICCSP.2016.7754396.
[26] S. Xiong and J. Bokor, "Sensitivity of Double-Gate and FinFET Devices to Process Variations," *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 2255–2261, 2003, doi: 10.1109/TED.2003.818594.
[27] S. Verma, S. L. Tripathi, and M. Bassi, "Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications," *Proc. 3rd Int. Conf. 2019 Devices Integr. Circuit, DevIC 2019*, no. August, pp. 84–88, 2019, doi: 10.1109/DEVIC.2019.8783754.
[28] W. P. Maszara and M. R. Lin, "FinFETs - Technology and circuit design challenges," *Eur. Solid-State Device Res. Conf.*, pp. 3–8, 2013, doi: 10.1109/ESSDERC.2013.6818808.
[29] A. Priydarshi and M. K. Chattopadhyay, "Low-Power and High-Speed Technique for logic Gates in 20nm Double-Gate FinFET Technology," *J. Phys. Conf. Ser.*, vol. 755, no. 1, 2016, doi: 10.1088/1742-6596/755/1/012055.
[30] S. Dwivedi and D. N. R. Prakash, "A Study on Recent Advancements in VLSI Technology using FinFETs," *Int. J. Innov. Res. Sci. Eng. Technol.*, vol. 12, no. 4, pp. 12788–12793, 2015, doi: 10.15680/IJIRSET.2015.0412120.
[31] T. A. Bhat, M. Mustafa, and M. R. Beigh, "Study of short channel effects in n-FinFET structure for Si, GaAs, GaSb and GaN channel materials," *J. Nano- Electron. Phys.*, vol. 7, no. 3, pp. 1–5, 2015.
[32] S. I. et al. . Shafiqul Islam et al., "A Comparative Study of Sub-10nm Si, Ge and GaAs n-Channel FinFET," *Int. J. Semicond. Sci. Technol.*, vol. 7, no. 1, pp. 1–6, 2017, doi: 10.24247/ijsstdec20171.
[33] C. Chugh, V. Narula, S. Lata, and B. Raj, "The effects of variation in geometry parameters on sub-50 nm finfet and their direct impact on finfet performance," *Proc. - 2nd Int. Conf. Intell. Circuits Syst. ICICS 2018*, no. October, pp. 184–187, 2018, doi: 10.1109/ICICS.2018.00045.
[34] A. Mahmood, W. A. Jabbar, Y. Hashim, and H. Bin Manap, "Effects of downscaling channel dimensions on electrical characteristics of InAs-FinFET transistor," *Int. J. Electr. Comput. Eng.*, vol. 9, no. 4, pp. 2902–2909, 2019, doi: 10.11591/ijece.v9i4.pp2902-2909.

[35] M. Bir, S. Gulshan, R. Singh, J. S. Sodhi, and J. S. Sawhney, “Advanced VLSI Technology : FinFET Technology,” *Jetir*, vol. 6, no. 6, pp. 64–68, 2019.

[36] M. S. Islam, M. S. Hasan, M. R. Islam, A. Iskanderani, I. M. Mehedi, and M. T. Hasan, “Impact of Channel Thickness on the Performance of GaAs and GaSb DG-JLMOSFETs: An Atomistic Tight Binding based Evaluation,” *IEEE Access*, vol. 9, pp. 117649–117659, 2021, https://doi.org/10.1109/ACCESS.2021.3106141.

[37] V. Kumar, R. Gupta, R. Preet, P. Singh, and R. Vaid, “Performance Analysis of Double Gate n-FinFET Using High-k Dielectric Materials,” *Int. J. Innov. Res. Sci. Eng. Technol.*, vol. 5, no. 7, pp. 13242–13249, 2016.